



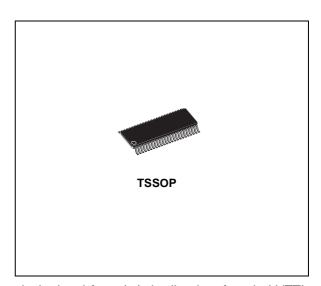
# HIGH SPEED PROTECTION SWITCH

- 24mA CMOS OUTPUT DRIVE CURRENT
- LVTTL INPUT THRESHOLDS
- CONTROLLED SKEW BETWEEN DATA AND CLOCK SIGNALS
- LVDS INPUT-OUTPUT UP TO 155 MHZ
- IMPROVED LATCH-UP IMMUNITY UP TO 300mA

#### **DESCRIPTION**

The STLVD112 is a low voltage differential to LVTTL signal converter with enhanced loop-back and crosspoint features. The synchronous design allows a phase alignment between a clock and its data; this means a better BER (Bit Error Rate) performance.

The advanced 0.35µm technology makes the STLVD112 suitable for data rates up to 200Mbit. The main application field is SDH/SONET telecom infrastructure. The STLVD112 flexible switch architecture makes it easy to implement multiple protection schemes in STM1 access systems. Thanks to the flexible multiplexing allowed, it becomes simple to redirect the data/clock signal coming from the faulty access card to the spare card. In normal mode the STLVD112 converts the differential data levels of the LVDS and related



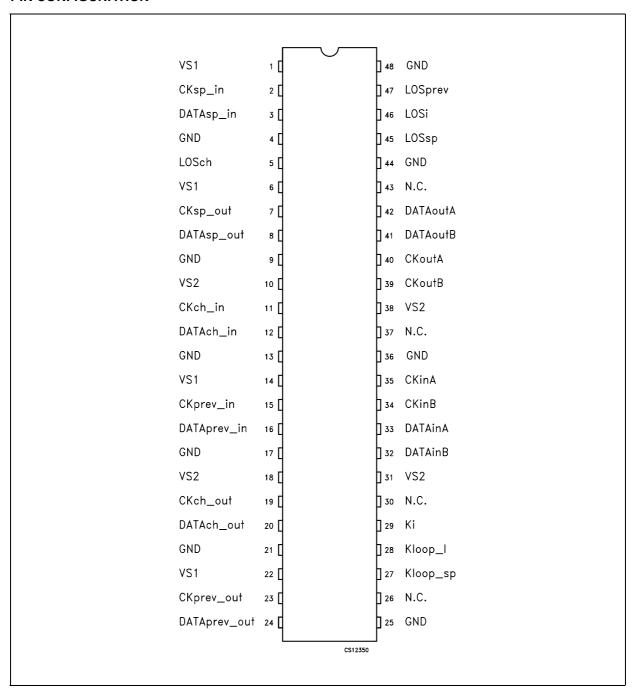
clock signal from (to) the line interface in LVTTL level signals to (from) the backpanel. In addition the switch functions prevent the equipment from line interface faults. In fact, it is possible to switch the signals coming from a different line interface to the local line interface or the signals from the local line interface to a different line interface.

#### **ORDERING CODES**

Туре	Temperature Range	Package	Comments
STLVD112BTR	-40 to 85 °C	TSSOP48 (Tape & Reel)	1000 parts per reel
STLVD112CTR	0 to 70 °C	TSSOP48 (Tape & Reel)	1000 parts per reel

April 2003 1/11

#### **PIN CONFIGURATION**



## **PIN DESCRIPTION**

PIN N°	SYMBOL	NAME AND FUNCTION
1, 6, 14, 22	VS1	Main Power Supply
2	CKsp_in	LVTTL Clock Input
3	DATAsp_in	LVTTL Data Input
4, 9, 13, 17, 21, 25, 36, 44, 48	GND	Ground
5	LOSch	Control Output
7	CKsp_out	LVTTL Clock Output
8	DATAsp_out	LVTTL Data Output
10, 18, 31, 38	VS2	Second Power Supply
11	CKch_in	LVTTL Clock Input
12	DATAch_in	LVTTL Data Input
15	CKprev_in	LVTTL Clock Input
16	DATAprev_in	LVTTL Data Input
19	CKch_out	LVTTL Clock Output
20	DATAch_out	LVTTL Data Output
23	CKprev_out	LVTTL Clock Output
24	DATAprev_out	LVTTL Data Output
26, 30, 37, 43	N.C.	Not Connected
27	Kloop_sp	Control Input
28	Kloop_I	Control Input
29	Ki	Control Input
32	DATAinB	LVDS Data Input -
33	DATAinA	LVDS Data Input +
34	CKinB	LVDS Clock Input -
35	CKinA	LVDS Clock Input +
39	CKoutB	LVDS Clock Output -
40	CKoutA	LVDS Clock Output +
41	DATAoutB	LVDS Data Output -
42	DATAoutA	LVDS Data Output +
45	LOSsp	Control Output
46	LOSi	Control Input
47	LOSprev	Control Input

## TRUTH TABLES FOR THE FIVE MUX

	OUTPUT		
Ki Kloop_sp Kloop_			DATA_out
LOW	Х	Х	DATAch_in
HIGH	Х	Х	DATAsp_in

	INPUTS		
Ki Kloop_sp		Kloop_i	DATAch_out
X	X	LOW	DATAin
Х	X	HIGH	DATAch-in

	INPUTS			
Ki	Kloop_sp	Kloop_i	DATAsp_out	
LOW	LOW	Х	DATAprev_in	
HIGH	LOW	X	DATA_in	
X	HIGH	X	DATAsp_in	

	OUTPUT		
Ki Kloop_sp		Kloop_i	LOSch
Х	X	LOW	LOSi
X	X	HIGH	LOW

	OUTPUT		
Ki	Ki Kloop_sp		LOSsp
LOW	LOW	X	LOSprev
HIGH	LOW	X	LOSi
Χ	HIGH	X	LOW

#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
VS1, VS2	Supply Voltage	-0.3 to 4.6	V
VS2	Supply Voltage	-0.3 to (VS1 + 0.3)	V
VI	DC Input Voltage	-0.3 to (VS1 + 0.3)	V
Vo	DC Output Voltage	-0.3 to (VS1 + 0.3)	V
lik	DC Input Diode Clamp Current	±20	mA
lok	DC Output Diode Clamp Current	±20	mA
Io	DC Output Current	±50	mA
$T_L$	Lead Temperature (10sec)	300	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

## **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
VS1, VS2	Supply Voltage	3 to 3.6	V
VS2	Supply Voltage	3 to (VS1 + 0.3)	V
V <sub>I</sub>	DC Input Voltage	0 to VS1	V
Vo	DC Output Voltage	0 to VS1	V
Тор	Operating Temperature	-45 to 85	°C
dt/dv	Maximum Input Rise and Fall Time	10	ns/V

**ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A=25^{\circ}C$  and  $V_{S1}$ ,  $V_{S2}=3.3V$ )

Symbol	Parameter	Test Conditions	Value			Unit
Symbol	Parameter	rest conditions	Min.	Тур.	Max.	Offic
V <sub>OL</sub>	Low Level Output Voltage	I <sub>OUT</sub> = 24 mA		0.2	0.4	V
V <sub>OH</sub>	High Level Output Voltage	I <sub>OUT</sub> = 24 mA	V <sub>SI</sub> -0.5	V <sub>SI</sub> -0.3		V
$V_{IL}$	Low Level Input Thresholds	$V_{OUT} = 0.1V \text{ or } V_{S1} - 0.1$	0		8.0	V
V <sub>IH</sub>	High Level Input Thresholds	$V_{OUT} = 0.1V \text{ or } V_{S1} - 0.1$	2		$V_{SI}$	V
I <sub>IN</sub>	Input Leakage Current	$V_{IN} = GND \text{ or } V_{CC}$	-1		1	μΑ
I <sub>CC</sub>	Quiescent Supply Current	$V_{IN}$ = GND or $V_{CC}$		15		mA
		$f_{CLOCK} = 155MHz$		110		

# **LVDS DRIVER ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at $T_A$ =25°C and $V_{S1}$ , $V_{S2}$ = 3.3V)

Symbol	Parameter	Test Conditions		Unit		
Syllibol		rest conditions	Min.	Тур.	Max.	Offic
V <sub>OD</sub>	Differential Output Voltage	$R_L = 100 \Omega$	247	364	454	mV
ΔV <sub>OD</sub>	Change in differential output voltage between logic states		-50		50	mV
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage		1	1.15	1.30	V
$\Delta V_{OC(SS)}$	Change in steady-state common- mode output voltage between logic State		-50		50	mV
$\Delta V_{OC(PP)}$	Peak-to-Peack common-mode output voltage			100	150	mV
I <sub>SC</sub>	Short Circuit Output Current	$V_{O(Y)}$ or $V_{O(Z)} = 0$	-24	-4		mA
		$V_{OD} = 0$			±12	
I <sub>OFF</sub>	Power Off Output Current	$V_{CC} = 0, V_{O} = 2.4V$	-1		1	μΑ

# **LVDS RECEIVER ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at $T_A$ =25°C and $V_{S1}$ , $V_{S2}$ = 3.3V)

Symbol	Parameter	Tool Oou dillone		Value		
	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>ITH+</sub>	Positive-going Differential Input Voltage Threshold				100	mV
V <sub>ITH-</sub>	Negative-going Differential Input Voltage Threshold		-100			mV
V <sub>ID</sub>	Magnitude of Differential Input Voltage		0.1		0.6	V
V <sub>IC</sub>	Common-mode Input Voltage		0.5  V <sub>ID</sub>		2.4-0.5  V <sub>ID</sub>    V <sub>CC</sub> -1	V

**LVDS SWITCHING TIMING CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A$ =25°C and  $V_{S1}$ ,  $V_{S2}$  = 3.3V)

Symbol	Parameter	Test Conditions  Value  Min. Typ.		Value			
Syllibol	Faranteter			Тур.	Max.	Unit	
t <sub>W</sub>	Minimum Pulse Width		<1			ns	

AC LVTTL IN LVTTL OUT (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A$ =25°C and  $V_{S1}$ ,  $V_{S2}$  = 3.3V)

Symbol	Parameter	Test Conditions	Value			Unit	
Symbol	Farameter	rest conditions	Min. Typ. Max		Max.		
t <sub>PLH</sub>	Propagation Delay Time, low-to-high-level output (50% to 50%)	Measured with $V_{IN}$ =0 to 2.5V, $f_{CLOCK}$ = 1MHz, $f_{DATA}$ = 0.5MHz	2.4	3.9	5.6	ns	
t <sub>PHL</sub>	Propagation Delay Time, high-to-low-level output (50% to 50%)	t <sub>r</sub> = t <sub>f</sub> = 0.4ns, +Duty Cycle=50% t <sub>PHL</sub> , t <sub>PLH</sub> are referred to output	2.5	4.2	5.3	ns	
t <sub>TLH</sub>	Transition Time, low-to-high-level output (10% to 90%)	clock transitions.	0.7	1.3	1.6	ns	
t <sub>THL</sub>	Transition Time, high-to-low-level output (90% to 10%)		0.7	1.1	1.3	ns	
f <sub>opr</sub>	Operative frequency		100	155	200	MHz	

**AC CONTROL OUTPUT** (LOSsp, LOSch) (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A$ =25°C and  $V_{S1}$ ,  $V_{S2}$  = 3.3V)

Councils and	Davamatav	Test Conditions	Value			Unit
Symbol	bol Parameter Test C	rest conditions	Min.	Тур.	Max.	Unit
t <sub>PLH</sub>	Propagation Delay Time, low-to-high-level output (50% to 50%)	Measured with $V_{IN}$ =0 to 2.5V, $f_{CLOCK}$ = 1MHz, $f_{DATA}$ = 0.5MHz	2.4	3.6	4.4	ns
t <sub>PHL</sub>	Propagation Delay Time, high-to-low-		2.4	3.4	4.2	ns
t <sub>TLH</sub>	Transition Time, low-to-high-level output (10% to 90%)	clock transitions.	0.9	1.9	2.3	ns
t <sub>THL</sub>	Transition Time, high-to-low-level output (90% to 10%)		0.7	1.0	1.2	ns

**AC LVTTL IN LVDS OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A$ =25°C and  $V_{S1}$ ,  $V_{S2}$  = 3.3V)

Cumbal	Parameter	Test Conditions	Value			Unit	
Symbol	Parameter	rest conditions	Min. Typ.		Max.		
t <sub>PLH</sub>	Propagation Delay Time, low-to-high-level output (50% to 50%)	Measured with $V_{IN}$ =0 to 2.5V, $f_{CLOCK}$ = 1MHz, $f_{DATA}$ = 0.5MHz	2.8	3.8	4.7	ns	
t <sub>PHL</sub>	Propagation Delay Time, high-to-low-		2.6	3.4	4.1	ns	
t <sub>TLH</sub>	Transition Time, low-to-high-level output (20% to 80%)	clock transitions.	0.4	0.5	0.6	ns	
t <sub>THL</sub>	Transition Time, high-to-low-level output (80% to 20%)		0.4	0.6	0.7	ns	
f <sub>opr</sub>	Operative frequency		100	155	200	MHz	

AC LVDS IN LVTTL OUT (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A$ =25°C and  $V_{S1}$ ,  $V_{S2}$  = 3.3V)

Symphol	Parameter	Test Conditions	Value			Unit
Symbol	Parameter	rest conditions	Min. Typ. Max		Max.	Onit
t <sub>PLH</sub>	Propagation Delay Time, low-to-high-level output (50% to 50%)	V <sub>DIFF</sub> = 400mV Measured with V <sub>ICM</sub> = 1.2 V,	4.3	5.6	6.9	ns
t <sub>PHL</sub>	Propagation Delay Time, high-to-low-level output (50% to 50%)	$f_{CLOCK} = 1MHz$ , $f_{DATA} = 0.5MHz$ $t_r = t_f = 0.4ns$ , +Duty Cycle=50%	4.1	5.4	6.7	ns
t <sub>TLH</sub>	Transition Time, low-to-high-level output (10% to 90%)	t <sub>PHL</sub> , t <sub>PLH</sub> are referred to output clock transitions	0.7	0.9	1.1	ns
t <sub>THL</sub>	Transition Time, high-to-low-level output (90% to 10%)		0.8	1.0	1.3	ns
f <sub>opr</sub>	Operative frequency		100	155	200	MHz

**LVTTL IN LVTTL OUT** ( $V_{CC}$  = 3 to 3.6V  $T_A$  = -45 to 80°C, unless otherwise noted. Typical values are at  $T_A$  = 25°C)

Symbol	Parameter	Test Conditions	Value			Unit
Symbol	Farameter	rest conditions	Min.	Offic		
t <sub>s</sub>	Setup Time	f = 10MHz, V <sub>ICM</sub> = 1.2 V	1			ns
t <sub>H-</sub>	Hold Time	$V_{DIFF} = 400 \text{mV},$ $V_{INTTL} = 0 \text{ to } 2.5 \text{V}$	1			ns

**LVTTL IN LVDS OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A$ =25°C and  $V_{S1}$ ,  $V_{S2}$  = 3.3V)

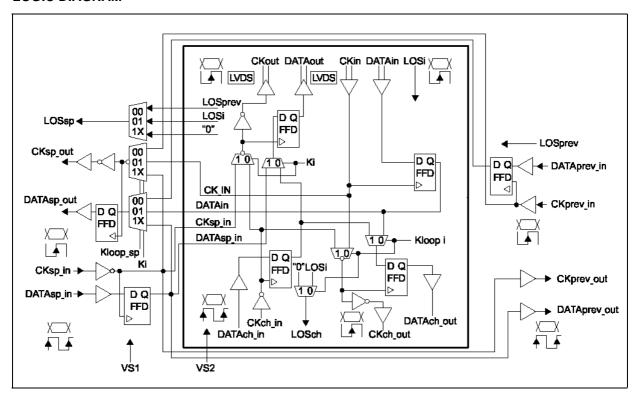
Symbol	Parameter	Test Conditions		Unit		
Symbol	raiametei	rest Conditions	Min.	Тур.	Max.	Onit
t <sub>s</sub>	Setup Time	f = 10MHz, V <sub>ICM</sub> = 1.2 V	1			ns
t <sub>H-</sub>	Hold Time	$V_{DIFF} = 400 \text{mV},$ $V_{INTTL} = 0 \text{ to } 2.5 \text{V}$	1			ns

**LVDS IN LVTTL OUT** (Over recommended operating conditions, unless otherwise noted. All typical values are at  $T_A$ =25°C and  $V_{S1}$ ,  $V_{S2}$  = 3.3V)

Symbol	Parameter	Test Conditions		Unit		
Symbol	Farameter	rest conditions	Min.	Тур.	Max.	Onit
t <sub>s</sub>	Setup Time	f = 10MHz, V <sub>ICM</sub> = 1.2 V	1.5			ns
t <sub>H-</sub>	Hold Time	$V_{DIFF} = 400 \text{mV},$ $V_{INTTL} = 0 \text{ to } 2.5 \text{V}$	1			ns

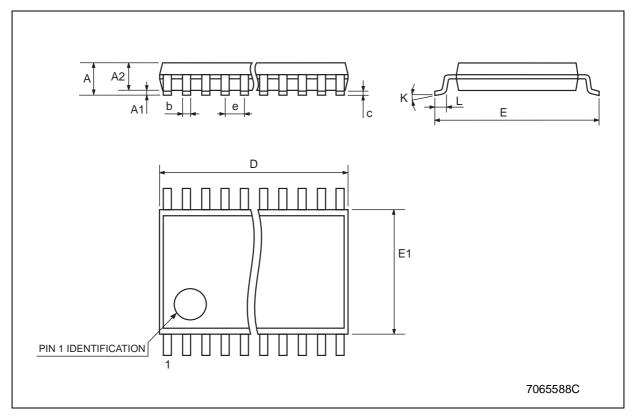
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#### LOGIC DIAGRAM



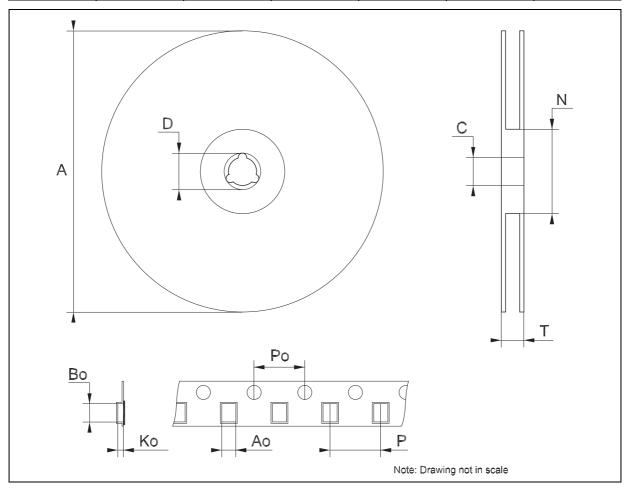
# **TSSOP48 MECHANICAL DATA**

DIM.	mm.			inch			
DIW.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
А			1.2			0.047	
A1	0.05		0.15	0.002		0.006	
A2		0.9			0.035		
b	0.17		0.27	0.0067		0.011	
С	0.09		0.20	0.0035		0.0079	
D	12.4		12.6	0.488		0.496	
E		8.1 BSC			0.318 BSC		
E1	6.0		6.2	0.236		0.244	
е		0.5 BSC			0.0197 BSC		
К	0°		8°	0°		8°	
L	0.50		0.75	0.020		0.030	



Tape & Reel TSSOP48 MECHANICAL DATA

DIM	mm.			inch			
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
А			330			12.992	
С	12.8		13.2	0.504		0.519	
D	20.2			0.795			
N	60			2.362			
Т			30.4			1.197	
Ao	8.7		8.9	0.343		0.350	
Во	13.1		13.3	0.516		0.524	
Ko	1.5		1.7	0.059		0.067	
Po	3.9		4.1	0.153		0.161	
Р	11.9		12.1	0.468		0.476	



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